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GROUP 2500

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit: 2512

Examiner: GIORDANA

Serial No. 08/654,760

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

VIA FACSIMILE 703 308 7722
Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
November 24, 1997

Attn: Examiner Giordana

SUPPLEMENTAL AMENDMENT

Dear Sir:

In response to the Office Action mailed , please amend the above identified case as follows.

IN THE DRAWINGS

Enclosed is a markup of Figure 33 for approval by the Examiner.

Remarks

The undersigned noticed, after filing the amendment in response to the Office action mailed 7/15/97 on 11/15/97, that one of the drawings showing a cross section of the finished device has an error. Specifically, the error is that bit line 122 is shown as shorting the P region acting as the transistor channel region to the N regions acting as

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the source and drain. This short occurs because the P-type channel region and the N-type source region are shown as coming to the surface which they should not do at least in the vicinity on the surface where the bit line will short them together. The undersigned believes that those skilled in the art will appreciate this fact, and, since Figure 5 shows a correct cross section of the completed device, no new matter issue is raised by this change.

All claims are believed to be in condition for allowance, and favorable action is earnestly solicited.

Respectfully submitted,

Ronald C. Fish

Ronald Craig Fish

Reg. No. 28,843

Tel 408 778 3624

FAX 408 776 0426

Dated: November 24, 1997

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FIG. 34
SECTION C-C'

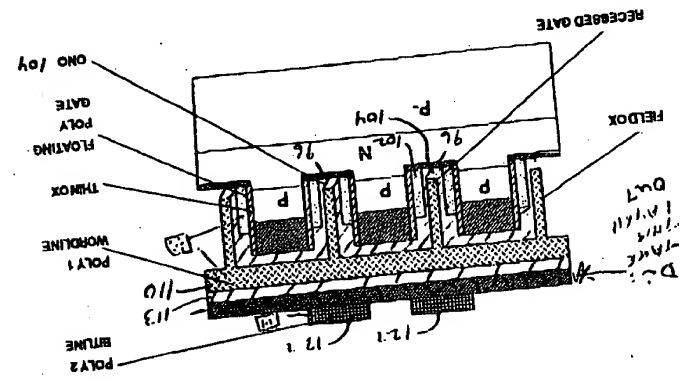


FIG. 33
SECTION A-A'

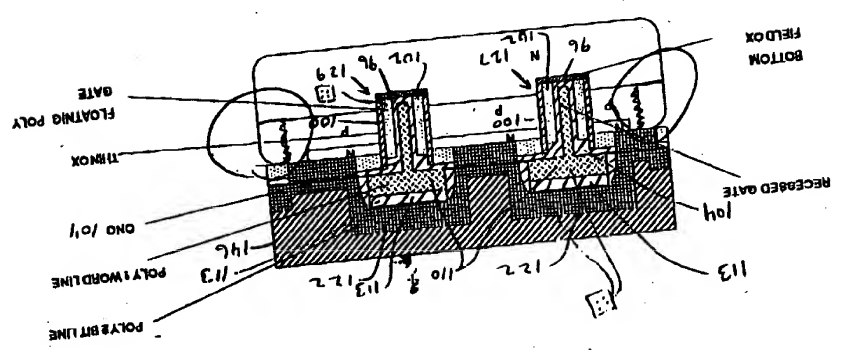


FIG. 32
TOP VIEW - FINISHED CELLS (FOUR)

